

REMARKS/ARGUMENTS

Claims 1-19 remain in the application. Claims 1-4, 7-12 and 16-19 stand rejected. Claims 5, 6 and 13-15 stand objected to as being dependent on other rejected claims, but are otherwise allowable.

1. Rejection of Claims 1, 2, 4, 7, 8, 11, 12 and 16-19 under 35 USC 102(b)

Claims 1, 2, 4, 7, 8, 11, 12 and 16-19 stand rejected under 35 USC 102(b) as being anticipated by Wright (US Pat. No. 5,264,740).

With respect to applicants' claim 1, the Examiner asserts that Wright teaches all of the limitations of applicants' claim. Applicants disagree. Claim 1 recites a "Boundary-Scan test receiver", including a comparator to receive signals "during board interconnect testing". The Examiner does not indicate where Wright teaches either of these. Applicants therefore believe that the Examiner has failed to make a prima facie case for rejecting claim 1, and that claim 1 should be allowed.

Claim 2 is believed to be allowable, at least, because it depends from claim 1.

With respect to applicants' claim 4, the Examiner asserts that Wright teaches a programmable hysteresis circuit with "a programmable hysteresis delay circuit" in FIG. 2. However, applicants can only find a generic "programmable hysteresis circuit 26" in Wright's FIG. 2. Applicants cannot find any indication that this circuit includes "a programmable hysteresis delay circuit". The circuit is certainly not identified by a text label. If the circuit is discussed in Wright's specification, applicants ask that the Examiner please indicate where. Applicants' claim 4 is believed to be allowable, at least, because it depends on claim 1, and for the additional reason given in this paragraph.

With respect to applicants' claim 7, applicant cannot find any mention by Wright of programmable inputs of a hysteresis circuit being linked by a scan chain. In fact, applicants cannot find *any* reference to a "scan chain" or "Boundary-Scan test".

The Examiner rejects claims 11, 12, 18 and 19 for the same reasons that claims 1 and 8 are rejected, and rejects claims 16 and 17 for the same reasons that claims 2 and 4 are rejected. However, claim 11 (from which the other claims depend) recites various actions that are to be taken as part of a Boundary-Scan test method. The final action is "executing a Boundary-Scan test". As previously indicated, applicants cannot find any mention by Wright of "Boundary-Scan test". Applicants therefore believe that the Examiner has failed to make a prima facie case for rejecting claims 11, 12, 18 and 19, and that these claims should be allowed.

Claim 8 is believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

2. Rejection of Claims 3, 9 and 10 under 35 USC 103(a)

Claims 5, 7, 8, 12, 18 and 20 stand rejected under 35 USC 103(a) as being unpatentable over Wright (US Pat. No. 5,264,740) in view of Jenkins et al. (US Pat. No. 5,610,545; hereinafter "Jenkins").

With respect to claims 3, 9 and 10, these claims are believed to be allowable, at least, because 1) they depend from claim 1, or are allowable over Wright alone for reasons similar to why claim 1 is believed to be allowable over Wright, and 2) Jenkins does not disclose that which is missing from Wright (see, section 1 of these Remarks/Arguments, *supra*). That is, Jenkins does not provide any mention of a "Boundary-Scan test receiver" or a comparator to receive signals "during board interconnect testing".

3. Allowability of Claims 5, 6 and 13-15

Claims 5, 6 and 13-15 stand allowable, but for their dependence on other rejected claims. Applicants thank the Examiner for indicating the allowability of these claims. However, applicants choose to leave these claims in their current form until


the Examiner has considered their above arguments for allowing the remainder of their claims.

4. Conclusion

In light of the amendments and remarks provided herein, applicants respectfully request the timely issuance of a Notice of Allowance.

Respectfully submitted,
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